Review of Self Tuning Methods for Direct Conversion Multistandard Transceivers

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***Abstract*—Integrated circuit fabrication technological processes affect error of Multistandard transceiver's components, thus aims to minimize such deviation. This paper analyzes modern multistandard wireless transceiver calibration methods: feedforward, feedback, hybrid and indirect. Main parameters to calibrate are: I/Q gain and phase imbalance, DC offset and second intercept point. For first time, relations between transceiver parameters, parameters to be calibrated and calibration methods are proposed.**

Keywords— integrated; circuit; multistandard transceiver; tuning; wireless

I. INTRODUCTION

Over last decades advancements of CMOS technology lead to fully integrated systems and increased range of applications. This led to exponential growth of devices that use wireless data transmission – mobile phones, smart phones, tablet PCs [1]. Moreover, as more and more wireless standards are integrated in devices, need of multiband, multistandard transceiver increases.

Multistandard direct conversion transceiver consists of direct conversion transmitter and direct conversion receiver. Transmitter part consists of I and Q channel digital to analogue converters (DAC), low pass filters (LPF), local oscillator (LO), mixers, power amplifier (PA) and band selection filter (BSF). Receiver part consists of BSF, low noise amplifier (LNA), mixers, LO, LPF, variable gain amplifiers (VGA) and analogue to digital converters. Signals are processed in digital signal processor.

Since CMOS process lacks of component parameter accuracy [2], this directly leads to overall operation of the transceiver. Thus, transceivers are meant to be calibrated [3], [4], so its parameters are tuned up to desired. As transceiver is specified by a series of parameter, Fig. 1 illustrates proposed relation between transceiver parameters, parameters to be calibrated and calibration methods [1], [3] – [58], [60] – [63].

II. METHODS OF SELF-CALIBRATION

Each transmitter and receiver architecture has its drawbacks associated with different unwanted processes, such as LO feed through, DC offset and so on. In such case, there is need of the calibration systems [3], [5]. This section reviews modern transceiver calibration methods and systems that help remove or suppress the mentioned problems.

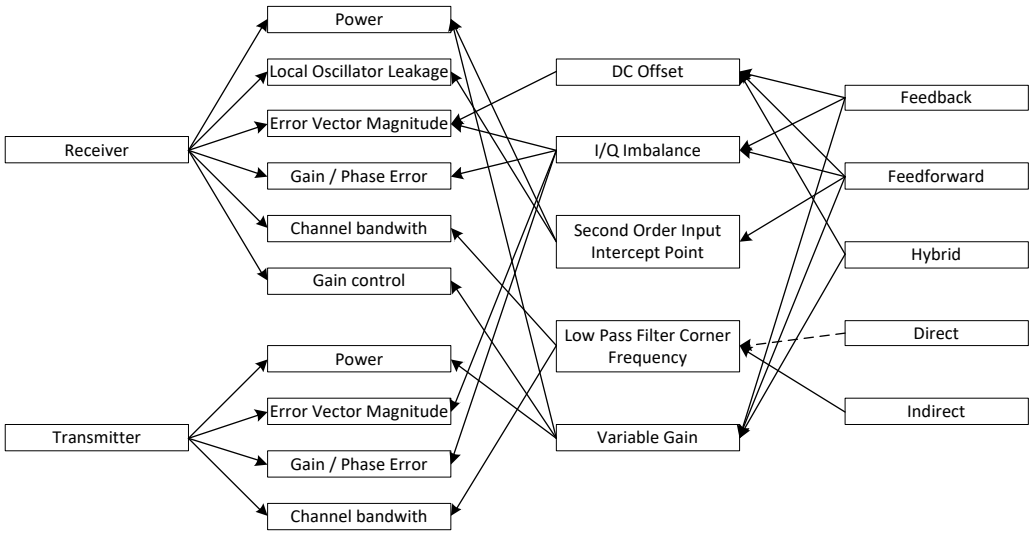

Fig. 1. Relations between transceiver parameters, parameters to be calibrated and calibration methods.

A. DC offset cancellation

One of the most severe problems in direct conversion receiver is sensitivity to DC offsets. DC offsets mainly arises from LO leakage or interference leakage. The insulation between the LO port and inputs of mixer and LNA is not infinite. This means that there exists finite amount of feed through from LO to input of the LNA and RF port of the mixer [6]. If the LO signal leaks to LNA, it is mixed with "real" LO signal and it produces a DC component. Similarly, if interference signal leaks from the LNA to LO port, it is multiplied by itself and also produce DC component. Similar, as in receiver, transmitter also suffers from LO leakage [7]. As illustrated in Fig. 2, mixer DC offset cancellation system consists of variable attenuator and phase shifter [16]. In order to eliminate DC offset, a bypass circuit is connected to RF port. Bypass circuit delivers the same signal amplitude as leakage signal, but its phase is shifted 180°.

Moreover, DC offset cancellation techniques are used in VGA calibration [8], [9], [10]. In receiver case, there is residual DC offset from mixer output, which also could be increased in LPF output. As gain of VGA is regulated to maximum desired amplitude, even small DC offset at input of the VGA could lead to heavy signal distortion at output [11], [12].

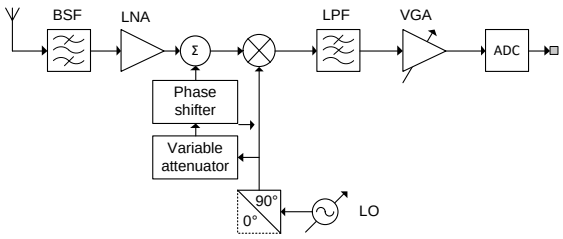

Fig. 2. Mixer DC offset cancellation feedback method

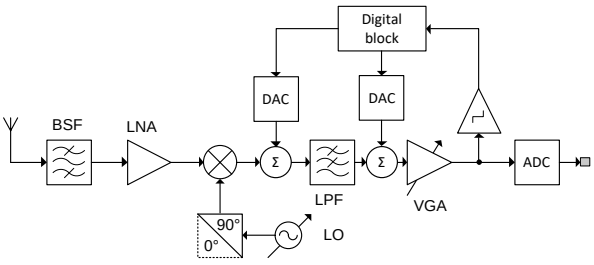

Fig. 3. Receiver VGA two step DC offset cancellation feedback method.

DC offset estimation and cancellation method for mixer is feedback [6], [13], [14] and for VGA are feedback [8], [9], [16], [18] and hybrid [15]. Most widely used VGA DC offset cancellation technique is feedback. Hybrid system is mixed with feedforward and feedback parts of system.

Feedback DC cancellation methods are split to simple and more complex, which includes ADCs, DACs and digital blocks for estimation of DC offset. As illustrated in Fig. 3, VGA DC offset cancellation system in receiver consists of comparator, digital block, which consists of computation block and registers, and DACs [17]. DC offset cancellation scheme consists of comparator, digital block and DACs for LPF and VGA input signal modification (Fig. 3).

Table 1 summarizes a part of the overviewed modern DC offset cancellation systems and their parameters. The major of modern calibration systems are employing feedback technique.

As seen from Table 1, DC offset cancellation in mixer block reduces DC offset up to 0.129 mV, or 45.3 dB. For VGA block, there are feedback and feedforward calibration techniques. Since different authors publish their simulation or measurement results using different input DC offset level, it is complicated to compare results.

A. I/Q imbalance calibration

An ideal I/Q transceiver, consists of I and Q branches, which analog circuits are same. However, in practice, due to IC manufacturing tolerances, it is not possible to perfectly balance I and Q branches. Moreover, analog components are affected by temperature variation, aging, etc. I/Q imbalance is mainly caused by the modulators, since I and Q branches have equal gain and 90 phase difference. However, other components – DACs or ADCs, filters and mixers also contribute in general to the imbalance effects [19].

I/Q imbalance calibration methods are off-line and on-line [20]. The I/Q imbalance causes noise between mirror signals, thus dynamic range of transceiver degrades. Suppression of image signal is specified as the image rejection ratio (IRR).

TABLE I. DIFFERENT DC OFFSET CANCELLATION SYSTEM COMPARISON

Reference	Year	Block	Technique	Process, µm	Before calibration, mV	After calibration, mV	Improvement, dB
[13]	2006	Mixer	Feedback	350	24	**0.129**	45.3
[6]	2007	Mixer	Feedback	350	–	2	–
[9]	2012	VGA	Feedback	180	110	**0.9**	41.7
[16]	2010	VGA	Feedback	180	327	1.6	46.2
[8]	2011	VGA	Feedback	180	135	4	30.6
[14]	2007	Mixer	Feedback	130	–	0.5	–
[18]	2010	VGA	Feedback	130	454	**3**	43.6
[15]	2015	VGA	Hybrid	130	11	**0.4**	28.8

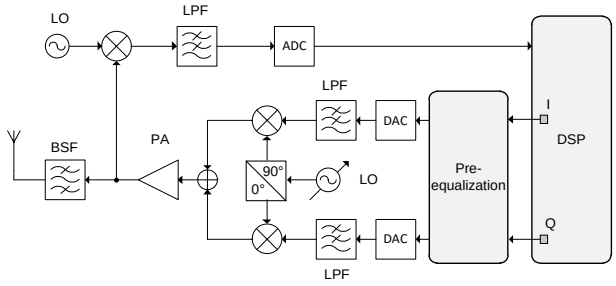

Fig. 4. Transmitter I/Q imbalance feedback calibration method.

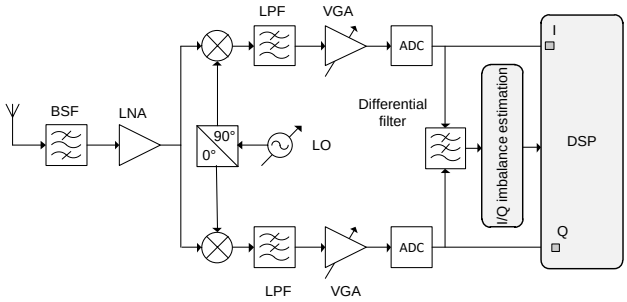

Fig. 5. Receiver I/Q imbalance feedforward calibration method.

TABLE II. DIFFERENT I/Q IMBALANCE CALIBRATION SYSTEM COMPARISON

Reference	Year	Block	Process, nm	IRR, dB
[29]	2015	Receiver	130	**60**
[31]	2011	Receiver	90	**55**
[28]	2013	Transmitter	65	**64**
[24]	2012	Receiver	65	56
[27]	2012	Receiver	65	55
[25]	2013	Transceiver	65	42
[30]	2017	Transceiver	65	47.5
[26]	2011	Transmitter	40	**55**

As illustrated in Fig. 4, transmitter calibration scheme consists of LO, mixer at RF PA output, LPF and ADC [21], [22]. DSP unit estimates imbalances of gain and phase shift in I and Q branches and pre-equalizes transmitted signal, thus I/Q imbalance is minimized.

Fig. 5 illustrates I/Q imbalance scheme at receiver end. Compensation scheme consists of differential filter and I/Q imbalance estimation circuit. Differential filter is used to remove transient response between I and Q branches [23]. Next, I/Q imbalance estimation circuit feeds DSP with signal correction data.

Table 2 summarizes a part of the overviewed modern I/Q imbalance calibration systems. Since different authors highlight different aspects of their proposal, comparing them is not very convenient. Main parameter of I/Q imbalance calibration systems is IRR.

As seen from Table 2, receiver with I/Q imbalance calibration system achieves IRR up to 60 dBm. The transmitter with I/Q imbalance calibration systems achieves IRR up to 64 dBm. I/Q calibration systems for both transmitter and receiver also are used. IRR of such systems reaches up to 47.5 dBm.

B. IIP2 calibration

Although the direct conversion receiver architecture is commonly used nowadays due to high integration level, low cost and simplicity, it has several issues [5], including second-order intermodulation (IM2) and third-order intermodulation (IM3). The most dominant source of IM2 is the down-conversion mixer. Balanced circuits with differential input and output, also symmetric layout is used to minimize the even-order distortion effects, but any mismatches in LO, like duty cycle and gain, make the differential circuit unbalanced and increases even-order distortion [32], [33] As every cellular system has IIP2 requirements [34] (see Table 3), receiver must meet them.

Adaptive IP2 calibration system is presented in Fig. 6. IP2 calibration system consists of common mode (CM) detector, LPF, ADC and least-mean square (LMS) filter [32], [33]. First branch of calibration system provides reference distortion signal. CM detector simplifies system as there is not needed use of signal squaring and LPF suppresses any out of band signal components. IM2 cancellation is performed entirely in the current domain, changing mixer output DC offset (Fig. 7) [33]. Table 4 summarizes a part of the overviewed IIP2 calibration systems.

As seen from Table 4, only 22% of overviewed receivers meet IIP2 requirements for LTE standard specifications before calibration, while after IIP2 calibration – 100%. Also, receivers fabricated using nanometre scale (90 nm and smaller) fabrication technology, has higher calibrated linearity, IIP2 of such receivers is >70 dBm.

TABLE III. IIP2 REQUIREMENTS OF CELLULAR SYSTEMS

Cellular system	Required IIP2, dBm
GSM	46
UMTS	49
LTE	62

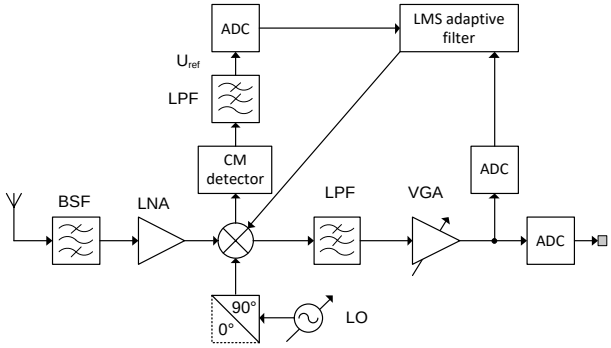

Fig. 6. Receiver adaptive IIP2 feedback calibration method.

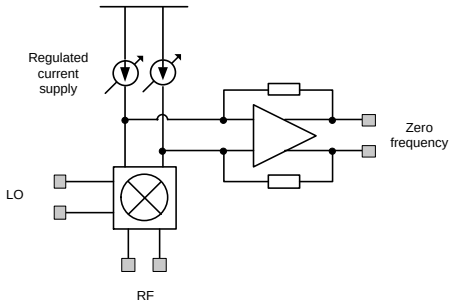

Fig. 7. Mixer output with regulated current supply.

TABLE IV. DIFFERENT IIP2 CALIBRATION SYSTEM COMPARISON

Reference	Year	Process, nm	Supply, V	LO frequency, GHz	IIP2 before calibration, dBm	IIP2 after calibration, dBm	IIP2 improvement, dBm
[35]	2008	180	1.8	3.5	47	68	19
[40]	2013	180	–	2.62	62	**83**	21
[33]	2008	130	1.5	–	58	74	16
[37]	2010	130	1.5	1.8	35	61	26
[39]	2011	130	1.5	1.8	36	60	24
[38]	2009	90	1.5	2.0	65	**90**	25
[36]	2008	65	1	1.98	55	**80**	25
[41]	2014	28	0.9	3.0–6.0	55	>**80**	25
[42]	2016	28	1.2	2.4	53	73	20

C. Low pass filter tuning

The accuracy of passband cut-off frequency is crucial in wireless applications. Active RC filters suffers from the RC time constant deviation with respect to processes, temperature and power supply voltage [43]. There are 3 main auto-tuning methods used for filter tuning: direct, indirect and using two identical filters [44].

Direct auto-tuning method works in offline mode – filter is disconnected from data transmission branch and connects to calibration system. This type of tuning method uses less IC area than other approaches, but since during filter calibration state transceiver cannot send or receive data, this approach is rarely used.

An auto-tuning system with two identical filters works in online mode – one filter is used for data transmission, while other is being calibrated. This type of tuning method is more likely to use more of IC area, since active RC filters more often are 4-6th order [45], [46], [47]. Such order filter, depending on used filter architecture, employs many components, and since tuning method uses two identical filters, overall number of components is twice as large.

As compromise between an off-line and large IC area using method, indirect tuning method [44], [48], [49] is used (Fig. 8). This tuning method works on-line, tunes dummy LPF, which is considered as identical to main LPF. It is possible to achieve same IC process mismatch in both filters if they are centred and are near as possible. Tuning scheme consists of frequency divider, comparator, resistor (or capacitor) matrix and D-type flip-flop. Most common, in LPF tuning systems, capacitor matrix is used for coarse tuning, or bandpass switching, while resistor matrix is used for fine bandpass tuning. Table 5 summarizes a part of the overviewed LPF calibration systems.

As seen from Table 5, LPF tuning range and tuning step does not depend on IC fabrication process node. Most recent work show, that tuning range reaches up to 45 %, while tuning step is about 1 % or smaller. It should be mentioned that reducing tuning step drastically increases IC area. Most of authors do not publish IC area for LPF tuning system.

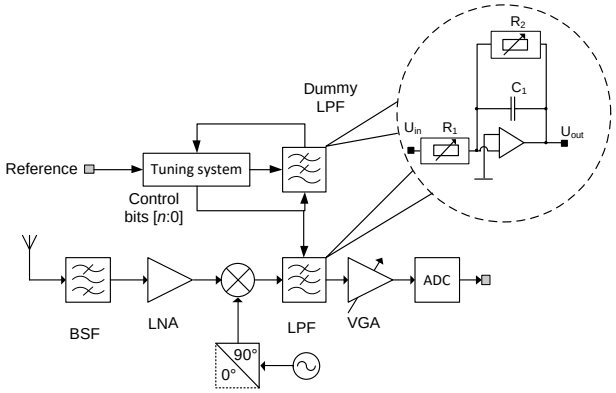

Fig. 8. Indirect LPF corner frequency tuning method.

TABLE V. DIFFERENT LPF CORNER FREQUENCY TUNING SYSTEM COMPARISON

Reference	Year	Process, nm	Supply, V	Corner frequency, MHz	Tuning range, %	Tuning step, %
[47]	2009	180	1.8	3.75	**40**	4
[51]	2012	180	1.8	0.25; 0.5; 1.0; 2.0	20	3
[49]	2016	180	1.8	10	30	**1**
[54]	2016	180	1.8	0.25	**40**	3.33
[50]	2011	130	1.5	0.2; 2.0	20	2.5
[53]	2016	130	1.3	0.06; 0.18	**30**	**2**
[44]	2017	65	1.2	10–60	**40**	**0.9**
[52]	2014	55	1	2.5	**45**	**3**

D. Automatic gain control

Automatic gain control is an essential function in modern wireless communication systems. Due to the complicated electromagnetic environment and uncertain distance from signal source, the received signal strength suffers from significant variation [55]. For maximum effective dynamic range of ADC, AGC is necessary. There are 3 main VGA AGC methods: feedback, feedforward and hybrid.

Most of the AGC systems employ two or three VGA [56]. Commonly, first VGA is used for coarse tuning, while second and third is used for fine tuning.

AGC system with feedforward or feedback loop consists of peak detector and gain control block, which is divided to coarse tuning circuitry and fine tuning circuitry (Fig. 9(a, b)) [57], [58]. Hybrid AGC consists of gain determinator and coarse and fine control unit (Fig. 9(c)), thus employs analogue and digital tuning [59]. Table 6 summarizes a part of the overviewed AGC systems.

As seen from Table 6, feedforward AGC method has fastest settling time and is within 0.25 – 0.8 μs range, but gain range does not exceed 22 dB, as well gain step varies from 2 to 3 dB/step. The feedback AGC method has far wider gain range, which varies from 40 to 89 dB, gain step varies from 1 to 3 dB/step, but settling time varies from 3.2 to 24 μs. Recent studies introduced hybrid AGC method, which employs both fast settling time, up to 3 μs, as well as high gain range, up to 96 dB and 1 dB/step gain step.

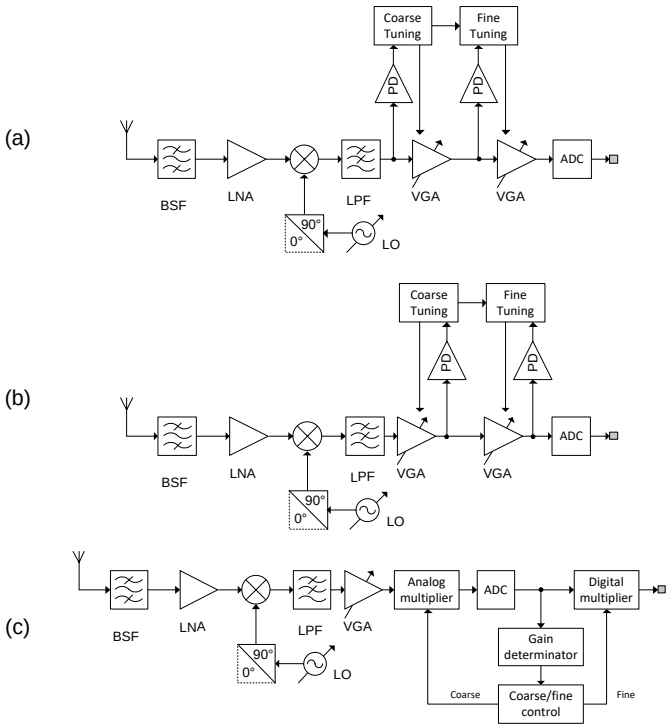

Fig. 9. AGC method, (a) – feedforward, (b) – feedback, (c) – hybrid.

TABLE VI. DIFFERENT AGC SYSTEM COMPARISON

Reference	Method	Year	Process, nm	Supply, V	Gain range, dB	Gain step, dB	Settling time, μs
[57]	Feedforward	2010	350	1.8	22	**2**	0.8
[61]	Feedforward	2008	350	1.8	21	3	**0.25**
[58]	Feedback	2009	250	1.8	54	1	3.2
[63]	Feedback	2006	180	1.8	40	**1**	**5.6**
[62]	Feedback	2010	180	1.8	60	2	<20
[64]	Feedback	2011	180	1.8	**89**	3	24
[60]	Hybrid	2014	180	1.7	49.3	**1**	–
[56]	Hybrid	2015	65	1	**96**	**1**	3

III. CONCLUSIONS

This paper has reviewed the most important parameters to be calibrated in modern transceivers. After analysis of 64 references, parameters to be calibrated in transceivers are DC offset, I/Q imbalance, IP2, LPF corner frequency and VGA gain. Moreover, each transceiver's parameter is calibrated using various methods: feedforward, feedback, hybrid, direct and indirect.

DC offset cancellation methods are feedback and hybrid. Modern DC offset calibration systems reduces DC offset up to 0.129, and improvement of DC offset reaches up to 46.2 dB.

Second most important parameter for calibration in modern transceivers is I/Q imbalance. I/Q imbalance calibration method for receiver is feedforward, while for transmitter – feedback. In modern transceiver, with I/Q imbalance calibration, IRR reaches up to 64 dB. Most of calibration systems employ DSP unit for I/Q imbalance calibration.

Every cellular standard has its own requirements for IP2. Main block for IP2 calibration is the mixer. In modern transceiver IIP2 after calibration reaches up to 90 dBm.

Low pass filter tuning methods are direct, indirect and using two identical filters. Most common LPF tuning method is indirect. While virtually corner frequency of filter can be tuned up to 0%, it requires large area of IC for large resistors. Recent works showed that corner frequency is tuned up to 0.8%, while tuning range can be achieved 45%.

An AGC system is not crucial in modern transceivers, but is recommended, since it leads to more accurate digitization of signal. AGC methods are feedforward, feedback and hybrid. Feedforward AGC method has fastest settling time, feedback method – wider gain range and smaller gain step and hybrid has average settling time, wide gain range and small gain step. Most recent works showed that hybrid AGC method reaches both wide gain range, up to 96 dB, and fast settling time, up to 3 μs.

REFERENCES

[1] A. Parssinen, "Multimode-multiband transceivers for next generation of wireless communications", 2011 Proceedings of the ESSCIRC (ESSCIRC), pp. 25-36, 2011.

[2] IBM, "Foundry technologies 180-nm CMOS, RF CMOS and SiGe BiCMOS", 2003.

[3] M. Onabajo and J. Silva-Martinez, Analog circuit design for process variation-resilient systems-on-a-chip. New York: Springer, 2012.

[4] B. Razavi, "Design considerations for direct-conversion receivers", IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 44, no. 6, pp. 428-435, 1997.

[5] R. Svitek and S. Raman, "DC offsets in direct-conversion receivers: characterization and implications", IEEE Microwave Magazine, vol. 6, no. 3, pp. 76-86, 2005.

[6] Q. Xu, X. Hu, Y. Jan, Y. Shi, F. Dai and R. Jaeger, "A Direct-Conversion Mixer with a DC-offset Cancellation for WLAN", 2007 IEEE Bipolar/BiCMOS Circuits and Technology Meeting, pp. 13-16, 2007.

[7] Y. Fang, Y. Jun, M. Heping, S. Yin and D. Foster, "A direct-conversion WLAN transceiver baseband with DC offset compensation and carrier leakage reduction", Journal of Semiconductors, vol. 31, no. 10, pp. 149-152, 2010.

[8] G. Huang, Y. Wu, C. Zhong and P. Lin, "A DC-offset cancellation circuit for PGA in baseband communication", 2011 IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS), pp. 1-4, 2011.

[9] X. Li, X. Le Cui, B. Wang and C. Lee, "A 100MHz PGA with DC offset cancellation for UWB receiver", 2012 IEEE 11th International Conference on Solid-State and Integrated Circuit Technology, pp. 1-3, 2012.

[10] J. Cheng, F. Huang, L. Wu, Y. Tian and N. Jiang, "A High-Linearity, 60-dB Variable Gain Amplicier with Dual DC-Offset Cancellation for UWB Systems", 2009 5th International Conference on Wireless Communications, Networking and Mobile Computing, pp. 1-4, 2009.

[11] F. Xiangning, C. Da and F. Yangyang, "A switch controlled resistor based CMOS PGA with DC offset cancellation for WSN RF chip", 2010 International Symposium on Signals, Systems and Electronics, pp. 1-4, 2010.

[12] F. Xiangning, S. Yutao and F. Yangyang, "A CMOS DC offset cancellation (DOC) circuit for PGA of low IF wireless receivers", 2010 International Symposium on Signals, Systems and Electronics, pp. 1-4, 2010.

[13] Oimins Xu, Xueqing Hu, Pens Gao, Jun Yan, Shi Yin, F. Dai and R. Jaeser, "A direct-conversion mixer with DC-offset cancellation for IEEE 802.11a WLAN receiver", 2006 IEEE International Symposium on Circuits and Systems, pp. 4, 2006

[14] Y. Furuta, T. Heima, H. Sato and T. Shimizu, "A Low Flicker-Noise Direct Conversion Mixer in 0.13 um CMOS with Dual-Mode DC offset Cancellation Circuits", 2007 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, pp. 265-268, 2007.

[15] X. Ken, C. Min, H. Xiaoyong, C. Zhijian and Z. Weiguo, "An automatic DC-Offset cancellation method and circuit for RF transceivers", 2015 IEEE 11th International Conference on ASIC (ASICON), pp. 1-4, 2015.

[16] Shuhei Yamada, O. Boric-Lubecke and V. Lubecke, "Cancellation techniques for LO leakage and Dc offset in direct conversion systems", 2008 IEEE MTT-S International Microwave Symposium Digest, pp. 1191-1194, 2008.

[17] Y. Huang, W. Li, S. Hu, R. Xie, X. Li, J. Fu, Y. Sun, Y. Pan, H. Chen, C. Jiang, J. Liu, Q. Chen, D. Qiu, Y. Qin, Z. Hong and X. Zeng, "A High-Linearity WCDMA/GSM Reconfigurable Transceiver in 0.13um CMOS", IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 1, pp. 204-217, 2013.

[18] Xiaojie Chu, Min Lin, Zheng Gong, Yin Shi and Fa Foster Dai, "A CMOS programmable gain amplifier with a novel DC-offset cancellation technique", IEEE Custom Integrated Circuits Conference 2010, pp. 1-4, 2010.

[19] A. Kiayani, L. Anttila, Y. Zou and M. Valkama, "Advanced Receiver Design for Mitigating Multiple RF Impairments in OFDM Systems: Algorithms and RF Measurements", Journal of Electrical and Computer Engineering, vol. 2012, pp. 1-16, 2012.

[20] J. Jacobus de Witt, "Modelling, Estimation and Compensation of Imbalances in Quadrature Transceivers", Ph.D. dissertation, Stellenbosch University, pp. 60-63, 2011.

[21] J. Luo, A. Kortke and W. Keusgen, "Joint calibration of frequency selective time variant I/Q-imbalance and modulator DC-offset error in broadband direct-conversion transmitters", 2009 International Conference on Communications, Circuits and Systems, pp. 255-259, 2009.

[22] M. Inamori, A. Bostamam, Y. Sanada and H. Minami, "IQ Imbalance Compensation Scheme in the Presence of Frequency Offset and Dynamic DC Offset for a Direct Conversion Receiver", VTC Spring 2009 - IEEE 69th Vehicular Technology Conference, pp. 1-5, 2009.

[23] Y. Xu, N. Qi, Z. Chen, B. Chi and Z. Wang, "A hybrid approach to I/Q imbalance self-calibration in reconfigurable low-IF receivers", 2012 IEEE International Symposium on Circuits and Systems, pp. 552-555, 2012.

[24] W. Yu, C. Cheang, P. Mak, W. Cheng, K. Un, U. Lok and R. Martins, "A Nonrecursive Digital Calibration Technique for Joint Elimination of Transmitter and Receiver I/Q Imbalances With Minimized Add-On Hardware", IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 60, no. 8, pp. 462-466, 2013.

[25] E. Lopelli, S. Spiridon and J. van der Tang, "A 40nm wideband direct-conversion transmitter with sub-sampling-based output power, LO feedthrough and I/Q imbalance calibration", 2011 IEEE International Solid-State Circuits Conference, pp. 424-426, 2011.

[26] Y. Xu, B. Chi, X. Yu, N. Qi, P. Chiang and Z. Wang, "Power-Scalable, Complex Bandpass/Low-Pass Filter With I/Q Imbalance Calibration for a Multimode GNSS Receiver", IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 59, no. 1, pp. 30-34, 2012.

[27] Y. Yin, B. Chi, Q. Yu, B. Liu and Z. Wang, "A 0.1-5GHz SDR transmitter with dual-mode power amplifier and digital-assisted I/Q imbalance calibration in 65nm CMOS", 2013 IEEE Asian Solid-State Circuits Conference (A-SSCC), pp. 205-208, 2013.

[28] M. Huang, Xiaofeng Liang, J. Guo and D. Chen, "A compact I/Q imbalance calibration technique for power-aware fully-integrated receiver without on-chip baseband processor", 2015 IEEE International Wireless Symposium (IWS 2015), pp. 1-4, 2015.

[29] J. Pang, S. Maki, S. Kawai, N. Nagashima, Y. Seo, M. Dome, H. Kato, M. Katsuragi, K. Kimura, S. Kondo, Y. Terashima, H. Liu, T. Siriburanon, A. Narayanan, N. Fajri, T. Kaneko, T. Yoshioka, B. Liu, Y. Wang, R. Wu, N. Li, K. Tokgoz, M. Miyahara, K. Okada and A. Matsuzawa, "24.9 A 128-QAM 60GHz CMOS transceiver for IEEE802.11ay with calibration of LO feedthrough and I/Q imbalance", 2017 IEEE International Solid-State Circuits Conference (ISSCC), pp. 424-425, 2017.

[30] M. Kitsunezuka, T. Tokairin, T. Maeda and M. Fukaishi, "A Low-IF/Zero-IF Reconfigurable Analog Baseband IC With an I/Q Imbalance Cancellation Scheme", IEEE Journal of Solid-State Circuits, vol. 46, no. 3, pp. 572-582, 2011.

[31] K. Dufrêne, "Analysis and Cancellation Methods of Second Order Intermodulation Distortion in RFIC Downconverion Mixers", Ph.D. dissertation, Universität Erlangen-Nürnberg, pp. 114-135, 2007.

[32] K. Dufrene, Z. Boos and R. Weigel, "Digital Adaptive IIP2 Calibration Scheme for CMOS Downconversion Mixers", IEEE Journal of Solid-State Circuits, vol. 43, no. 11, pp. 2434-2445, 2008.

[33] E. Atalla, A. Bellaouar and P. Balsara, "IIP2 requirements in 4G LTE handset receivers", 2013 IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS), pp. 1132-1135, 2013.

[34] S. Rodriguez, A. Rusu, L. Zheng and M. Ismail, "CMOS RF mixer with digitally enhanced IIP2", Electronics Letters, vol. 44, no. 2, p. 121, 2008.

[35] M. Vahidfar and O. Shoaei, "A High IIP2 Mixer Enhanced by a New Calibration Technique for Zero-IF Receivers", IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 55, no. 3, pp. 219-223, 2008.

[36] Y. Feng, G. Takemura, S. Kawaguchi, N. Itoh and P. Kinget, "A low-power low-noise direct-conversion front-end with digitally assisted IIP2 background self calibration", 2010 IEEE International Solid-State Circuits Conference - (ISSCC), pp. 70-71, 2010.

[37] D. Kaczman, M. Shah, M. Alam, M. Rachedine, D. Cashen, L. Han and A. Raghavan, "A Single–Chip 10-Band WCDMA/HSDPA 4-Band GSM/EDGE SAW-less CMOS Receiver With DigRF 3G Interface and {+} 90 dBm IIP2 ", IEEE Journal of Solid-State Circuits, vol. 44, no. 3, pp. 718-739, 2009.

[38] Y. Feng, G. Takemura, S. Kawaguchi, N. Itoh and P. Kinget, "Digitally Assisted IIP2 Calibration for CMOS Direct-Conversion Receivers", IEEE Journal of Solid-State Circuits, vol. 46, no. 10, pp. 2253-2267, 2011.

[39] P. Jiang, Z. Lu, R. Guan and J. Zhou, "All-Digital Adaptive Module for Automatic Background IIP2 Calibration in CMOS Downconverters With Fast Convergence", IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 60, no. 7, pp. 427-431, 2013.

[40] B. van Liempd, J. Borremans, E. Martens, S. Cha, H. Suys, B. Verbruggen and J. Craninckx, "A 0.9 V 0.4-6 GHz Harmonic Recombination SDR Receiver in 28 nm CMOS With HR3/HR5 and IIP2 Calibration", IEEE Journal of Solid-State Circuits, vol. 49, no. 8, pp. 1815-1826, 2014.

[41] D. Danilovic, V. Milovanovic, A. Cathelin, A. Vladimirescu and B. Nikolic, "Low-power inductorless RF receiver front-end with IIP2 calibration through body bias control in 28nm UTBB FDSOI", 2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), pp. 87-90, 2016.

[42] M. Heping, Y. Fang, S. Yin and D. F, "A multi-standard active-RC filter with accurate tuning system", Journal of Semiconductors, vol. 30, no. 9, p. 095011, pp. 1-4, 2009.

[43] K. Kiela, "Design of Integrated Analog Filters for Wireless Communication Systems", Ph.D. dissertation, Vilnius Gediminas Technical University, pp. 37-123, 2017.

[44] Jinup Lim, Youngjoo Cho, Kyungsoo Jung, Jongmin Park, Joongho Choi and Jaewhui Kim, "A wide-band active-RC filter with a fast tuning scheme for wireless communication receivers", Proceedings of the IEEE 2005 Custom Integrated Circuits Conference, pp. 637-640, 2005.

[45] Yu-Chih Chen, Wei-Hao Chiu and Tsung-Hsien Lin, "A 120-MHz active-RC filter with an agile frequency tuning scheme in 0.18 um CMOS", 2008 IEEE International Symposium on VLSI Design, Automation and Test (VLSI-DAT), pp. 208-211, 2008.

[46] C. Fan, Y. Lu and C. Mao, "Design of a Chebyshev low pass filter with automatic frequency calibration", 2009 Asia Pacific Conference on Postgraduate Research in Microelectronics & Electronics (PrimeAsia), pp. 121-124, 2009.

[47] T. Oshima, K. Maio, W. Hioe and Y. Shibahara, "Novel automatic tuning method of RC filters using a digital-DLL technique", IEEE Journal of Solid-State Circuits, vol. 39, no. 11, pp. 2052-2054, 2004.

[48] K. Kiela, M. Jurgo and L. Kladovščikov, "Integrated Analogic Filter Tuning System Design", Mokslas - Lietuvos ateitis, vol. 8, no. 3, pp. 308-314, 2016.

[49] Chen Jiang, Renzhong Xie, Weinan Li, Yumei Huang and Zhiliang Hong, "Reconfigurable low pass filter with Automatic Frequency Tuning for WCDMA and GSM application", 2011 9th IEEE International Conference on ASIC, pp. 1066-1069, 2011.

[50] J. Gao, H. Jiang, L. Zhang, J. Dong and Z. Wang, "A programmable low-pass filter with adaptive miller compensation for zero-IF transceiver", 2012 IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS), pp. 226-229, 2012.

[51] Tien-Yu Lo and Chi-Hsiang Lo, "1-V 365 uW 2.5-MHz Channel Selection Filter for 3G Wireless Receiver in 55-nm CMOS", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 22, no. 5, pp. 1164-1169, 2014.

[52] R. Wang, M. Lin, H. Wang and S. Sun, "A widely tunable active-RC complex filter for multi-mode wireless receivers with automatic frequency tuning", IEICE Electronics Express, vol. 13, no. 18, pp. 1-11, 2016.

[53] M. Yen, C. Wu and H. Chen, "An automatic frequency tuning loop for the low pass filter of 400–800 MHz Spectrum sensing system", 2016 IEEE 5th Global Conference on Consumer Electronics, pp. 1-2, 2016.

[54] Y. Song, X. Yu, Z. Jin and B. Chi, "A 49-dB DR wide locking range hybrid AGC for an ISM-band receiver in 0.18 um CMOS", 2014 IEEE International Symposium on Radio-Frequency Integration Technology, pp. 1-3, 2014.

[55] J. Dong, H. Jiang, Z. Weng, J. Zheng, C. Zhang and Z. Wang, "A fast AGC method for multimode zero-IF/sliding-IF WPAN/BAN receivers", 2015 IEEE International Symposium on Circuits and Systems (ISCAS), pp. 1310-1313, 2015.

[56] J. Pérez, B. Calvo and S. Celma, "A High-Performance CMOS Feedforward AGC Circuit for a WLAN Receiver", IEEE Transactions on Industrial Electronics, vol. 57, no. 8, pp. 2851-2857, 2010.

[57] J. Alegre, S. Celma, B. Calvo, N. Fiebig and S. Halder, "SiGe Analog AGC Circuit for an 802.11a WLAN Direct Conversion Receiver", IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 56, no. 2, pp. 93-96, 2009.

[58] Genesis Microchip Inc., "Hybrid automatic gain control (AGC)", US7222037 B2, 2007.

[59] Y. Song, X. Yu, Z. Jin and B. Chi, "A 49-dB DR wide locking range hybrid AGC for an ISM-band receiver in 0.18 um CMOS", 2014 IEEE International Symposium on Radio-Frequency Integration Technology, pp. 1-3, 2014.

[60] J. Alegre, B. Calvo and S. Celma, "A high performance CMOS feedforward AGC circuit for wideband wireless receivers", 2008 IEEE International Symposium on Industrial Electronics, pp. 1657-1661, 2008.

[61] Xiaoman Wang, Baoyong Chi and Zhihua Wang, "A Low-Power High-Data-Rate ASK IF Receiver With a Digital-Control AGC Loop", IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 57, no. 8, pp. 617-621, 2010.

[62] O. Jeon, R. Fox and B. Myers, "Analog AGC Circuitry for a CMOS WLAN Receiver", IEEE Journal of Solid-State Circuits, vol. 41, no. 10, pp. 2291-2300, 2006.

[63] A. Ximenes and J. Swart, "Analog automatic gain control (AGC) CMOS WLAN direct conversion receiver (DCR)", 2011 SBMO/IEEE MTT-S International Microwave and Optoelectronics Conference (IMOC 2011), pp. 185-190, 2011.