JOHN C. LIOBE, PhD

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CURRENT STATUS

Advis, Inc., Director of Engineering, 2008 – Present

- Fabless semiconductor startup company based in Rochester, NY
- Developer of novel sensor technologies
- Core technologies partially based on my graduate research

My role:

- *Chief architect of **DS Sentry™,** an ultra-low power acquisition and post-processing circuit for piezoelectric and capacitive sensors, which are utilized in such applications as machine and surveillance monitoring and intelligence gathering.*
- *Manage a team of five to eight hardware and software engineers.*
- *Responsible for all aspects of this product from the refinement of the initial idea through IC development and testing and full product development.*
- *SBIR/STTR/BAA proposal writing towards the end of additional funding procurement*
- *Create all technical marketing materials related to the DS Sentry™, including datasheets, presentations, and whitepapers.*
- *Maintain EDA-related software including Cadence, Matlab, Xilinx, Centos, RedHat, and Solaris*
- *Architected and maintain Advis's IT infrastructure.*

University of Rochester, Electrical and Computer Engineering, Postdoctoral Research Fellow, 2007 – Present

My role:

- *Mentor PhD students towards solving technical issues related to the DS Sentry™ as well as a novel high-resolution, low-noise, high-dynamic range CMOS image sensor, which is also being developed at Advis.*
- *Investigate novel signal processing and circuit techniques to improve low-light and high-light response of image sensor in the most efficient manner possible.*
- *Teach graduate/undergraduate courses in IC analog and digital design and test: Intro to VLSI and Advanced Digital Design.*

TEACHING INTERESTS

Analog IC Design

RF IC Design

VLSI Testing Methodologies
Logic Design
Two-dimensional Imaging Techniques
FPGA-based Digital System Design

RESEARCH INTERESTS

Mixed-signal/RF IC design
Analog signal processing techniques
CMOS image sensors
RF testing methodologies
Subthreshold/low-power analog design
Analog/Mixed-signal/RF DFT and BiST
Built-in Current Sensors
I_{DDQ}/I_{DDT} testing
Clock generation design and test
IR ROICs

EDUCATION

University of Rochester: **Ph.D.** in Electrical and Computer Engineering, April 2007
Dissertation title: *Novel Embedded Testing Methodology for Mixed-Mode Integrated Systems*
Advisor: Dr. Martin Margala
- Developed novel on-chip solutions for testing the integrated circuits contained in all modern cell phones as well as other wireless devices.

University of Rochester: **M.S.** in Electrical and Computer Engineering, May 2004

University of Rochester: **B.S.** in Electrical and Computer Engineering, May 2003
(Honors, with Distinction)

Simon School of Business: Completed coursework in the following classes: Technical Entrepreneurialship, Data Analysis, and Corporate Accounting.

PROFESSIONAL EXPERIENCE

Present	**Director of Engineering,** ADVIS, Inc., Rochester, NY
Present	**Postdoctoral Research Fellow**, ECE Department, University of Rochester, Rochester, NY
2003 – 2007	**Research Assistant**, Microelectronics Design and Test Laboratory, University of Rochester
2007	**Visiting Scientist**, NXP Semiconductors, Caen, FR
Summer 2006	Summer Intern, Harris Corp., RF Division, Rochester, NY
Summer 2005/2004	Summer Research Intern, IBM TJ Watson Research Center, Yorktown Heights, NY
Summer 2005	Senior Accounting Intern, Moore Capital Management, NY, NY
2005 – Present	Co-Founder of Innotech Education Services, Pittsburgh, PA

ACADEMIC HONORS

Fulbright Specialist Candidate (Awarded April 2012)
Semiconductor Research Corporation Student Research Fellow (Sept. 2004- August 2006)
Charles Merriam Teaching Assistant Award (April 2004)
Runner-up for Best Paper Award at NATW (May 2005)

INVITED TUTORIALS/PRESENTATIONS (6)

October 2006/07/08	Co-Presenter (w/ Sule Ozev [Univ. of Arizona] and Martin Margala [UMASS-Lowell]) at the *International Test Conference*, Santa Clara, CA, TUTORIAL TITLE: *Design for Testability for RF Circuits and Systems*.
April 2006	Wireless Test Workshop (In conjunction with VLSI Test Workshop) TITLE: *Novel BIT Solution for Mixed-Mode Integrated Systems*
Sept. 2006	Known Good Die Test Workshop, Napa, CA TITLE: *Towards the Test Compaction of RF/AMS Integrated Systems Utilizing Novel Sensor Designs*
August 2006	Infineon AG, Munich, Germany TITLE: *Towards the Test Compaction of RF/AMS Integrated Systems*

GRANT-BASED FUNDING

SBIR/STTRs (4):

- ***Readout Integrated Circuit (ROIC) Architecture Development for Remotely Piloted Aircraft (RPA) Imaging Sensors***, DoD (Air Force), $150K.
- ***Smart Infrared Focal Plane Arrays and Advanced Electronics***, DoD (MDA), $150K.
- ***Real Time Adaptable ROIC for Improved Power and Performance Optimization in Imager Systems***, DoD (Army), $150K.
- ***Development of an Integrated Power Line Sentry,*** DoE, $100K.
- ***High Performance Direct Photo-digital Coversion Readout Integrated Circuit for Corrugated Quantum Well Focal Plane Arrays,*** DoD (Army), $70K.
- ***Development of Sigma Delta-based Readout Integrated Circuit for Strained Layer Superlattice Photodetectors,*** DoD (Air Force), $100K.

Industrial/Government Collaborations (3):

- ***Technology Comparison for Image Sensing Applications in Standard CMOS and Silicon-on-Glass Materials,*** Corning, $100K.

- ***A 21st Century Approach to Electronic Device Reliability***, MURI (Office of Naval Research), $500K.
- ***DFX Solutions for PLLs on Advanced Digital Processes,*** Intel, $300K.

PUBLICATIONS

Refereed Journal Papers (11):

[1] Z. Gao, **J. Liobe**, Z. Ignjatovic, and M. Bocko, "Feedback Sigma-Delta Image Sensors: Theory, Modeling and Design," *IEEE Transactions on Circuits and Systems I (TCAS-I),* issue 99, pp. 1-13, April 2013.

[2] Zhe Gao, **John C. Liobe**, Zeljko Igjnatovic, and Mark F. Bocko, "CMOS Image Sensor Utilizing Both Sigma-Delta and SAR ADC with Pixel-by-Pixel Gain Control," *Submitted to IEEE JSSC*, Jan. 2012.

[3] **J. Liobe**, E. Moule, M. Balon, J. Small, Z. Ignjatovic, and M. Bocko, "DS Sentry™: An Ultra-low Power Dynamic Signal Processing Circuit with Noise-resilient 18-bit ΣΔ ADC," *Submitted to IEEE Sensors Journal*, Sept. 2010.

[4] E. Moule, **J. Liobe**, M. Balon, J. Small, M. Fiscella, Z. Ignjatovic, and M. Bocko, "A 1.2Mpixel CMOS Image Sensor Employing Oversampled Techniques for Low-light, Low-power Applications," *Submitted to IEEE Sensors Journal*, April 2011.

[5] **J. Liobe**, S. Soro, M. Balon, Z. Ignjatovic, and M. Bocko, "An Ultra-low Power Analog Front End for Capturing the Spectral Content from Piezoelectric and Capacitive Sensors," *Submitted to IEEE Sensors Journal*.

[6] **J. Liobe** and M. Bocko, "A Novel, Low-cost DFT," *Submitted to IEEE Signal Processing Letters*.

[7] J. Small, E. Moule, **J. Liobe**, M. Balon C. Meyer, I. Knausz, Z. Ignjatovic, and M. Bocko, "1.2 Mpixel CMOS Image Sensor for Ultra-low Power and Low-light Applications," *Submitted to IEEE Sensors Journal*, Sept. 2010.

[8] **J. Liobe** and M. Margala, "Novel Process and Temperature-Stable, IDD Sensor for the BIST Design of Embedded Digital, Analog, and Mixed-Signal Circuits," IEEE Transactions on Circuits and Systems I, vol. 54, no. 9, pp. 1900 - 1915, 2007

[9] **J. Liobe**, R. Geisler, and M. Margala, "A Novel Application of FM-ADC towards the Self-Calibration of Phase-Locked Loops," IEEE TCAS-I, Issue 55, Vol. 9, pp. 2491 – 2504, 2008.

[10] K. A. Jenkins, W. Rhee, **J. Liobe**, and H. Ainspan, "Experimental Analysis of the Effect of Substrate Noise on PLL Performance," IBM, IEEE TCAS-II, Issue 54, Vol. 9, pp. 1900 – 1915, 2007.

Conference Papers Appearing in Printed Proceedings (Reviewed, 19):

[1] T. Soyata and **J. Liobe**, "pbCAM: Probabilistically-banked Content Addressable Memory," *IEEE International SOC Conference (SOCC)*, 12-14 Sept. 2012, pp. 27-32.

[2] Zhe Gao, **John C. Liobe**, Zeljko Igjnatovic, and Mark F. Bocko, "Indirect-Feedback Sigma-Delta Image Sensor Readout Utilizing SAR ADC for Startup Phase," *Submitted to IEEE CICC*, Oct. 2013.

[3] Zhe Gao, **John C. Liobe**, Zeljko Igjnatovic, and Mark F. Bocko, "AV Sentry: a high-dynamic range, ultra-low noise ROIC for the visible through the infrared bandwidths," *Accepted to IEEE SPIE Defense, Security, and Sensing*, May 2013.

[4] Zhe Gao, **John C. Liobe**, Zeljko Igjnatovic, and Mark F. Bocko, "Noise Model of Indirect-Feedback Sigma-Delta Image Sensors," *Accepted to IEEE ISCAS*, May. 2013.

[5] **J. Liobe**, Z. Ignjatovic, and M. Bocko, "DS Sentry™: an acquisition ASIC for smart, micro-power sensing applications," Proceedings of SPIE, April 2011.

[6] **J. Liobe**, Z. Ignjatovic, and M. Bocko, "Ultra-low Overhead Signal Acquisition Circuit for Piezoelectric and Capacitive Sensors," Proceedings of MWCAS, pp. 33 – 36, May 2008.

[7] **J. Liobe** and M. Margala, "Wideband, Process and Temperature-stable IDD Sensor for AMS Testing Applications," University of Rochester, 2007.

[8] **J. Liobe** and M. Margala, "Defect-based, Process-tolerant Testing Solution for CMOS LNAs and Mixers," University of Rochester, 2007.

[9] **J. Liobe** and M. Margala, "Embedded ADC-based RFIC Testing Solution for CMOS Front-Ends," University of Rochester, 2007.

[10] **J. Liobe** and M. Margala, "Fault diagnosis of a GHz CMOS LNA using high-speed ADC-based BIST," Proceedings of the IEEE International Workshop on Current and Defect Based Testing, pp. 85 - 89, April 2004.

[11] **J. Liobe** and M. Margala, "Fault Threshold Analysis and Fault Coverage Study of GHz LNAs Using ADC- based Test," Proceedings of the Design Automation and Test in Europe, in preparation for the 1st IEEE RF/Multi-Gigahertz Test Workshop (in conjunction with DATE Conference), Feb. 2004.

[12] K. A. Jenkins, W. Rhee, **J. Liobe**, and H. Ainspan, "Experimental analysis of the effect of substrate noise on PLL performance," Proceedings of the Digest of Papers of the Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, pp. 54 - 57, Jan. 2006.

[13] **J. Liobe** and M. Margala, "Novel Process and Temperature-Stable BICS for Embedded Analog and Mixed-Signal Test," Proceedings of the IEEE International On-Line Testing Symposium, pp. 231 - 236, July 2007.

[14] **J. Liobe** and K. A. Jenkins, "A circuit-sensitive methodology for evaluating substrate noise," Proceedings of the Digest of Papers of the IEEE Radio Frequency integrated Circuits Symposium, pp. 657 - 661, June 2005.

[15] **J. Liobe**, X. Yunan, and M. Margala, "Non-intrusive testing methodology for CMOS RF LNAs," Proceedings of the Digest of Papers of the IEEE Radio Frequency integrated Circuits Symposium, pp. 653 - 656, June 2005.

[16] **J. Liobe** and M. Margala, "Deep-submicron CMOS design of high-performance low-power flash/folding analog-to-digital converters," Proceedings of the Canadian Conference on Electrical and Computer Engineering pp. 1629 - 1632, May 2004.

[17] Q. Diduck, **J. Liobe**, S. Ali, and M. Margala, "Process tolerant calibration circuit for PLL applications with BIST," Proceedings of the IEEE International Symposium on Circuits and Systems, pp. 2477 - 2480, May 2006.

[18] R. Geisler, **J. Liobe**, and M. Margala, "Process and Temperature Calibration of PLLs with BiST Capabilities," Proceedings of the IEEE International Symposium on Circuits and Systems, pp. 3864 - 3867, May 2007.

[19] M. Wieckowski, **J. Liobe**, Q. Diduck, and M. Margala, "A new test methodology for DNL error in flash ADCs," Proceedings of the IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, pp. 582 - 590, Oct. 2005.

Unpublished (1):

[1] Q. Diduck and **J. Liobe**, "Temperature Resistant Ramp Generator for Analog Testing," University of Rochester, Unpublished, 2005.

REVIEW ACTIVITIES

Journals:

2010 – Present	International Journal of Communication Systems
2008 – Present	IEEE Transactions on VLSI Systems
2008 – Present	IEEE Journal of Circuits, Systems, and Computers
2007 – Present	Journal of Solid-State Circuits
2003 – Present	Journal of Electronic Testing: Theory and Applications

2003 – Present Transactions of Circuits and Systems I

Conferences:
2010 – Present IEEE GLSVLSI
2003 – Present IEEE Defect and Fault Test Symposium
2003 – Present IEEE VLSI Test Symposium
2003 – Present IEEE International Test Conference
2003 – Present IEEE Design and Test in Europe
2003 – Present IEEE International Symposium on Circuits and Systems

Societies and Affiliations

2001 – Present Member of IEEE (Institute of Electrical Engineers)
2003 – Present Member of the Test Technology Education Program
2000 – Present Sigma Chi Fraternity Brother

Additional Skills and Achievements

- Foundational in Italian and Spanish; compentancy in Lithuanian.
- University of Rochester Assistant Water Polo Coach
- Big Brothers and Big Sisters STEM mentor

Interests

- Training for triathalons
- Competing in water polo tournaments
- Kitesurfing the Finger Lakes and the Outer Banks
- Playing the piano
- Reading historical fiction

References

Available upon request.